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(54) Process for the digital generation of a complex baseband signal

(57) A process is proposed that is used for the digital generation of a complex baseband signal from a real, sampled baseband signal. The process includes a sample-and-hold device 1, an A/D convertor 2, a frequency generator 3, a frequency divider 4 and a digital filter 6. The real baseband signal s(t) is sampled at a first clock frequency F and converted into a series of digital numbers with the aid of the A/D convertor 2. The digital numbers are fed to the all-pass filters of a recursive polyphase filter 6, whereby a digital number is filtered by each all-pass filter in each cycle of a second clock frequency F_c calculated from F. After filtering, the digital numbers are multiplied by specified coefficients in processor 8 and then added to obtain in-phase and quadrature components of the real baseband signal.

Application is to "frequency-hopping" systems.

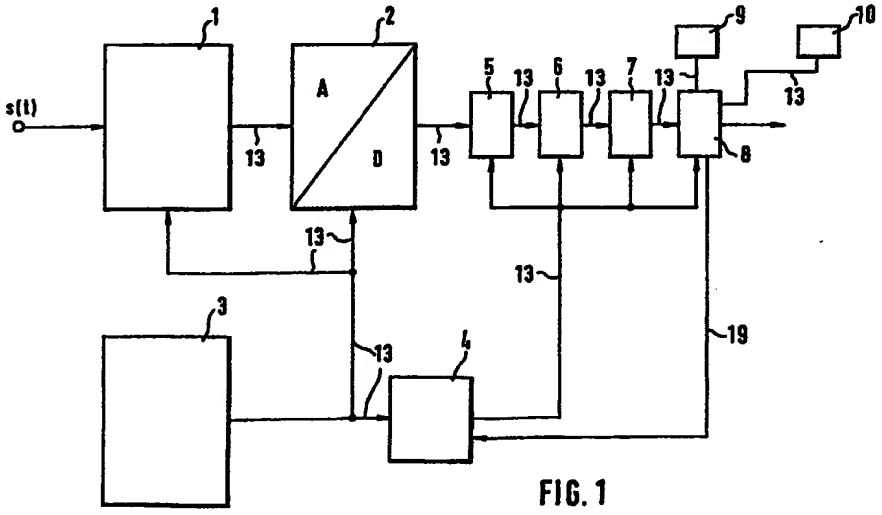

FIG. 1

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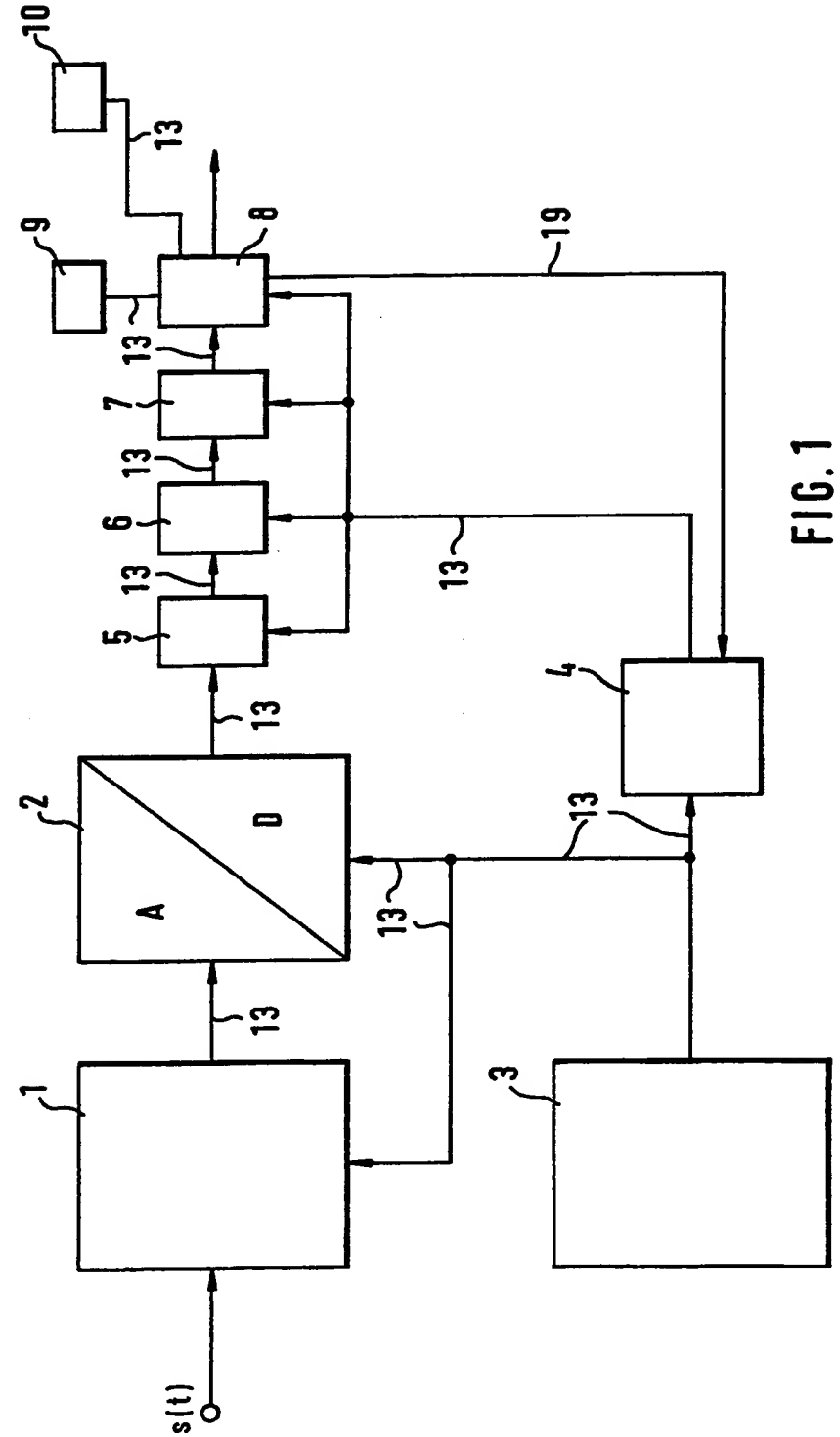

FIG. 1

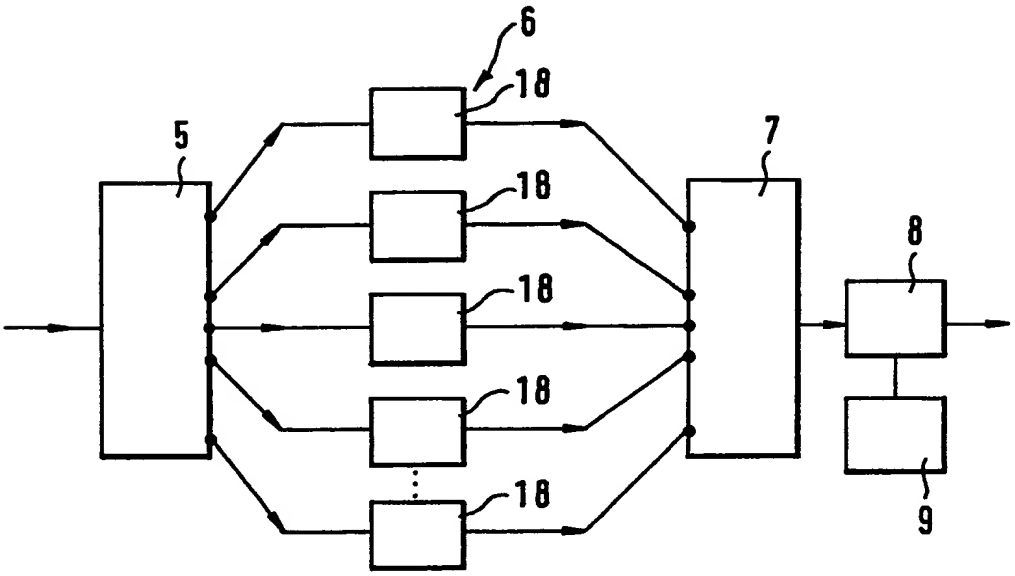

FIG. 2

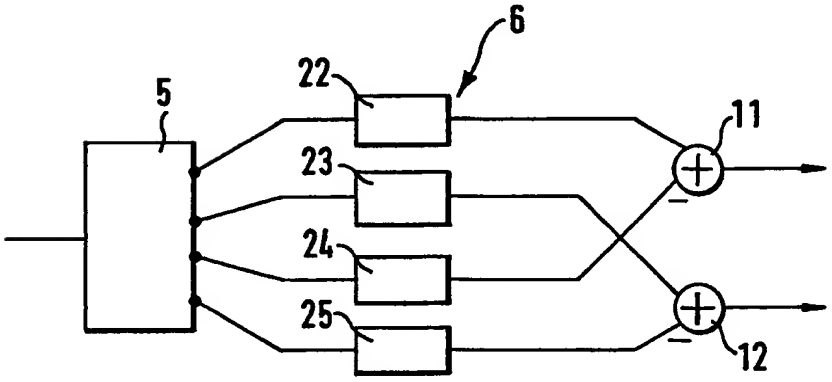

FIG. 3

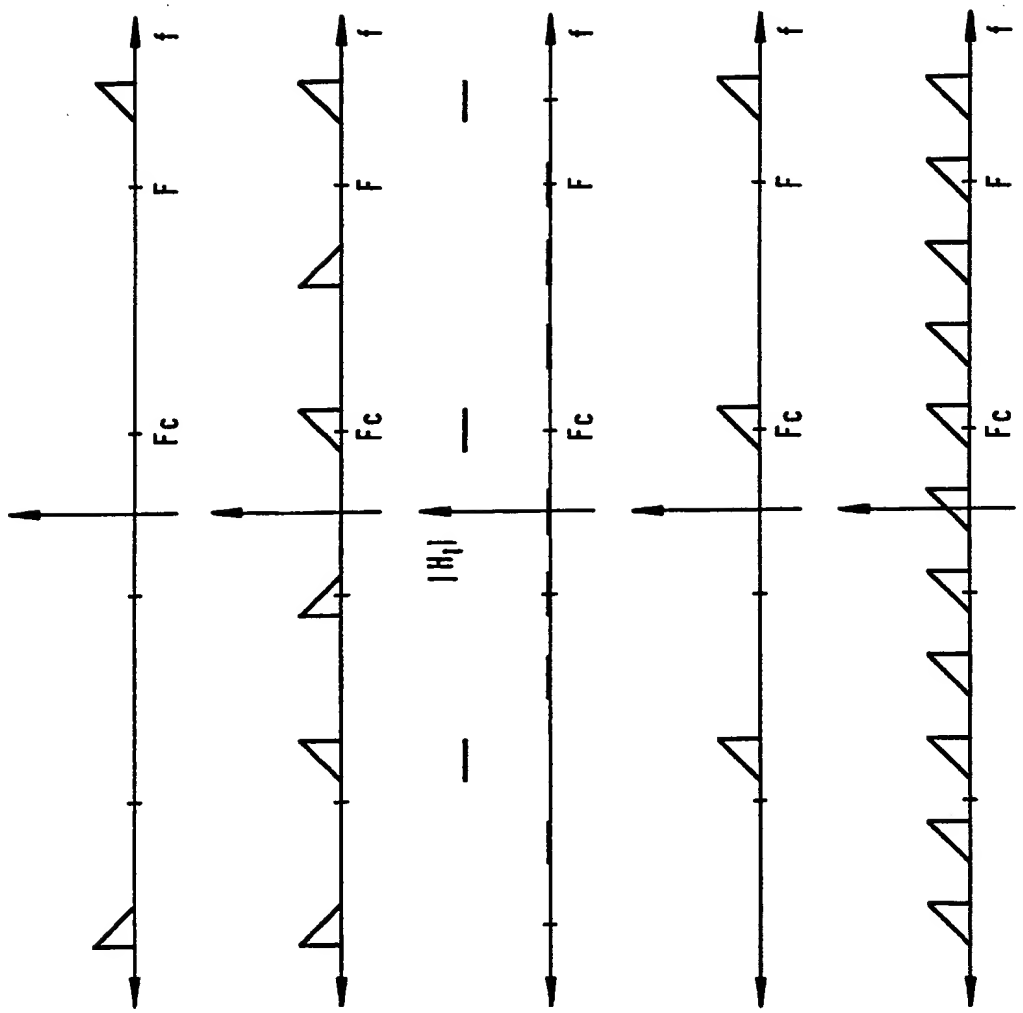

FIG.4a

FIG.4b

FIG.4c

FIG.4d

FIG.4e

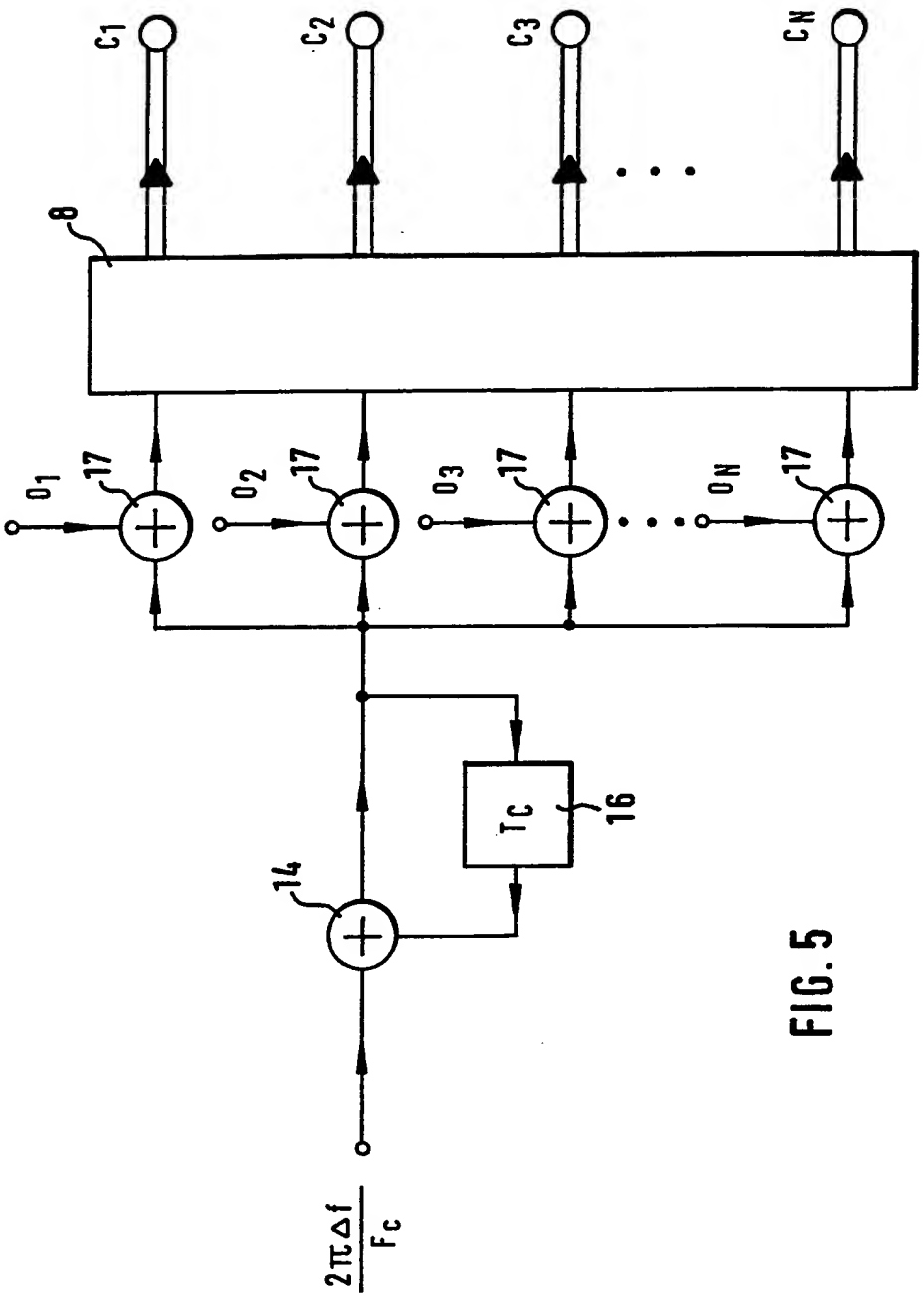

FIG. 5

Process for the digital generation of a complex baseband signal

State-of-the-art

The invention is based on a process for the digital generation of a complex baseband signal according to the form of the main claim. In a known analogue solution to this problem, the real baseband signal is first modulated with two channels with quadrature carriers and the signals are then passed through low-pass filters. The quality of this complex baseband conversion very much depends on the uniformity of the transfer functions in the channels. The two analogue low-pass filters are thus subject to the requirements for highest possible image frequency rejection with very stringent demands on the uniformity of the transfer function (magnitude and phase). In practice, the interference terms in this type of processing cannot be reduced below about -30 dB.

Furthermore, it is known that uniformity of both channels can be obtained by the use of digital signal processing. A high quality of conversion therefore results. Proposals for the digital generation of in-phase and quadrature components are known from the publications of L.E. Pellon: "A Double Nyquist Digital Product Detector for Quadrature Sampling", Transactions on Signal Processing, Vol. 40, No. 7, July 1992, and of W. Rosenkranz: "Quadrature Sampling of FM Bandpass Signals - Implementation and Error Analysis", Digital Signal Processing 87, Elsevier Science, 1987. Due to the use of the process steps: mixing with quadrature carriers and low-pass filtering in both channels, these methods are relatively costly.

Advantages of the invention

By contrast, the process according to the invention with the characterising features of the main claim has the advantage that only one processing channel is needed, so that signal mixing followed by low-pass filtering can be dispensed with. In this case, the complex bandpass filter for filtering the digital numbers can be clocked in an advantageous manner with the sampling rate of the complex baseband signal. Furthermore it is an advantage if the complex baseband signal is constructed with the aid of a polyphase filter, followed by multiplication with a factor C_K that results from frequency-shifting in the polyphase filter, and then addition. This simplifies the signal processing.

In an advantageous manner, the factor C_K with which the digital number is multiplied, is specified as an exponential function in relation to the control variable K which describes the Kth filter of a polyphase filter, and the clock frequency F_c. A shift in the frequency of the polyphase filter by L units of the second clock frequency F_c is thus achieved in a simple manner.

A particular form of the process consists in setting the number N of filters to a multiple of four and the constant L to a quarter of the number N of filters. This reduces the multiplication of filtered numbers with the factors C_K to a multiplication with the values +1 and -1.

The method used has the advantage that the in-phase components of the real baseband signal can be simply determined as a first sum of the digital numbers filtered by the filters with even control variable K, and the quadrature components of the real baseband signal determined as a second sum of the digital numbers filtered by the filters with odd control variable.

Designing the polyphase filter with all-pass filters is an advantage since all-pass filters are well suited to this type of signal processing. It is advantageous that the coefficients of the all-pass filters are represented with a shorter word length compared to other implementations.

Multiplication of the factors C_K before multiplication with the filtered numbers with a complex series that is specified in relation to a determined frequency deviation Δf, makes it possible to carry out a digital frequency correction simultaneously with the digital filtering in a simple manner.

The use of the factor C_K that in relation to the constant L that describes the shift in frequency of the polyphase filter by L units of the second clock frequency F_c, makes it possible to implement an immediate channel changeover by changing the constant L by whole values.

Drawing

An embodiment of the invention is shown in the drawing and described in more detail in the following description. Figure 1 shows an arrangement for the digital generation of a complex baseband signal, Figure 2 a polyphase filter, Figure 3 a special form of the polyphase filter, Figure 4 frequency spectra and Figure 5 a schematic block diagram for automatic frequency correction.

Description of the embodiment

Figure 1 shows a block diagram of the invention. A sample-and-hold device 1 is connected to the input of an analogue/digital converter 2 via a data line 13. The output of the A/D converter 2 leads via a data line 13 to the input of a multiplexer 5. This in turn is connected via a data line 13 to a polyphase filter 6, from which a data line 13 leads to a demultiplexer 7. The demultiplexer 7 is connected to the

central processor 8 via a data line 13. Via a data line 13, the central processor 8 has access to a memory 9. The central processor 8 is connected via a data line to an input unit 10. A clock generator 3 is connected to the clock input of the sample-and-hold device 1 and to the analogue/digital converter 2 and via a clock converter 4 to the multiplexer 5, the polyphase filter 6, the demultiplexer 7 and to the central processor 8. The central processor 8 is connected to the clock converter 4 via a further data line 19.

In Figure 1 a real bandpass signal s(t) is fed to the sample-and-hold device 1. A first clock frequency F is fed from the clock generator 3 to the sample-and-hold device 1. The sample-and=hold device 1 passes sampling values to the A/D converter 2. A first clock frequency F is fed from the clock generator 3 to the A/D converter 2. The A/D converter 2 passes a series of digital numbers to a multiplexer 5. The multiplexer 5 supplies the series of digital numbers to the filters of the polyphase filter 6. Polyphase filters are known from R.E. Crochiere, L.R. Rabiner, "Multirate Digital Signal Processing", Prentice Hall, 1983. The clock generator 3 supplies the first clock frequency F to a clock converter 4. The clock converter 4 determines a second clock frequency F_c according to the formula $F_c = F/N$, where F is the first clock frequency and N is a constant that is fed to the clock converter 4 by the central processor 8 via the further data line 19. The value for the constant N is passed to the central processor 8 via the input unit 10 and stored in the memory 9. The clock converter 4 passes the second clock frequency F_c to the multiplexer 5, the polyphase filter 6, the demultiplexer 7 and the central processor 8 via data lines 13. In the process a digital number is filtered from each filter of the polyphase filter 6 in one cycle of the second clock frequency F_c. The multiplexer 5 distributes the digital numbers in succession according to their chronological order to the filter of the polyphase filter 6.

The digital numbers filtered by the filters of the polyphase filter 6 are fed to the demultiplexer 7. The demultiplexer 7 passes the filtered numbers to the central processor 8, in the chronological order in which the digital data were fed to the multiplexer 5.

The central processor 8 executes a control program stored in the memory 9. According to the specified control program, the digital numbers of the central processor 8 are multiplied by the factors C_K stored in the memory 9 and are added in the prescribed manner. The in-phase and quadrature components of the baseband signal are obtained in this way, and then output.

Figure 2 shows a block diagram of a polyphase filter 6 that is constructed from a number N of filters 18 connected in parallel. Preferably, these filters 18 are designed as all-pass filters. All-pass filters are known, for example, from W. Schlüßler, "Digital Signal Processing, Vol. 1, Springer Verlag, 1988, and from A. Fettweis, "Wave Digital Filters, Theory and Practice", Proceedings IEEE, Vol. 25, No. 2, 1986. Figure 2 shows schematically that the multiplexer 5 feeds the digital numbers in their chronological order to the filters 18 of the polyphase filter 6, i.e. a digital number is processed by each filter 18 in each cycle of the second clock frequency F_c. A number N of digital numbers is fed again in the next frequency cycle to the filters 18 of the polyphase filter 6.

After filtering, the filters 18 of the polyphase filter 6 pass the filtered digital numbers to the demultiplexer 7. The demultiplexer 7 arranges the filtered digital numbers according to their chronological order and passes the filtered digital numbers to the central processor 8.

Figure 3 shows a particular form of the polyphase filter 6, in which the number N of filters is set at four. In this case a first, a second, a third and a fourth filter 22, 23, 24, 25 are arranged in parallel.

If the constant L that is taken into account when determining the factor c_K is now set to a quarter of the number N of the filters 18 of the polyphase filter 6, i.e. L = 1, then this gives $c_K = j^{k-1}$ for the factors, where j is the imaginary unit and K the control variable which designates the filter 18. It follows from this that the in-phase and quadrature components can be determined by a simple addition or subtraction.

The in-phase components of the baseband signals are obtained for the form of the polyphase filter 6 illustrated in Figure 3, if the digital number filtered by the first filter 22, and that filtered by the third filter 24 are fed to a first adder 11 and added, the digital number filtered by the third filter 24 receiving a negative sign. The quadrature components of the baseband signal are obtained by feeding the digital number filtered by the second filter 23 and the digital number filtered by the fourth filter 25 to a second adder 12, and added, the digital number filtered by the fourth filter 25 receiving a negative sign. A particularly simple form of digital filtering is achieved with the arrangement described.

Figure 4a represents a spectrum of a real bandpass signal. Figure 4b shows the spectrum of the real sequence sampled by a suitably-fast sample-and-hold device 1 at the sampling rate of the first clock frequency F. The digital, complex bandpass filter required for the generation of the complex baseband signal is shown schematically in Figure 4c. The lines drawn in Figure 4c designate the respective passbands or stop bands relevant to the design of the filter. The passbands that the complex bandpass filter is to have are identified by bars. The use of such a filter results in a filtered signal whose spectrum is shown schematically in Figure 4d, and which, by under-sampling with the factor N, finally produces the complex baseband signal with the sampling rate of the second sampling frequency F_c.

Figure 5 shows schematically the determination of the coefficients C_K, that are used for calculating the frequency response $H_L(w)$ of a complex bandpass filter, where an automatic frequency correction and a rapid channel changeover are achieved simultaneously. The complex series $S_o(n) = e^{-j2\pi n\Delta f/F_c} = e^{-jQ(n)}$ is generated by feeding the value $(2\pi\Delta f/F_c)$ to a loop with a time-delay element 16 and to a modulo 2 adder 14. The variable n designates the clock cycle. The time-delay element delays the signal by one clock cycle $T_c = 1/F_c$ and supplies it again to the modulo 2 adder 14. The resulting series Q(n) is fed to a further adder 17. In this example a number N of additional adders 17 is arranged - the same number as filters in the polyphase filter 6. The elements of the series with constant O_K are added in these additional adders 17, the variable K ranging from 1 to N. The coefficients O_K are defined as follows: $O_K = 2\pi(K-1)L/N$, where $K = 1, \ldots, N$.

The arguments of the exponential function $C_k(n) = e^{-j(O_k+Q(n))}$ required for determining the coefficients are thus specified. The sum $O_K+Q(n)$ is fed to the central processor 8 which determines the coefficients C_K, which are needed for producing the polyphase filter 6, from the sine and cosine tables stored in the memory 9.

A special embodiment is explained below with the aid of the Figures 1 to 4.

The circuit illustrated in Figure 1 is used to generate the digital in-phase and quadrature components of a complex baseband signal. The sampling rate of the complex baseband signal is designated as the second sampling frequency F_c. The sampling rate of the analogue/digital converter 2 is designated as the first sampling frequency F. The first sampling frequency F is made a whole multiple of the second sampling frequency F_c:

$F = N \times F_c(1)$, where the constant N designates a whole number greater than or equal to 2. Adjacent channel suppression is then only possible if the constant N is made greater than or equal to three. The following relationship applies between the centre frequency F_0 of the real bandpass signal s(t) and the first clock frequency F:

$F_0 = m \times F + L \times F_c \quad (2)$.

Here the constant *m* is a whole number and the constant L a value between (-(N-1)/2) and ((N-1)/2). To comply with the sampling theorem, the second sampling frequency F_c must be greater than or equal to the bandwidth of the bandpass signal. The relationship (2) represents a generalization of the known "quarter period sampling", as described by W. Rosenkranz, "Quadrature Sampling of FM bandpass Signals...", Digital Signal Processing 87, Elsevier Science. If these conditions are met, then the procedure illustrated in Fig. 4a to 4e for generating the complex baseband signal with the aid of a suitable choice of digital filter, can be used. In this embodiment constant N is specified as 4, constant *m* as 1 and constant L also as 1.

The real bandpass signal s(t), whose spectrum is shown in Figure 4a, is fed to the sample-and-hold device 1. Sampling is effected at the first clock frequency F that is applied to the sample-and-hold device 1 by the clock generator 3. A sampled, real series that is illustrated in Figure 4b, is generated by sampling from the real bandpass signal. To generate the complex baseband signal a digital complex band-pass filter is required, whose passbands and stop bands are arranged as shown in Figure 4c. The complex bandpass filter can be designed with the centre frequency $L \times F_c$ by shifting a real, so-called prototype low-pass filter. The limiting frequency of this low-pass filter should be half the bandwidth of the bandpass signal. A suitable structure for producing such a low-pass filter is a recursive polyphase filter 6 with a number N of

filters 18, as shown in Figure 2. The transfer function H(w) of the polyphase filter 6 is:

$$H(w) = 1/N \sum_{K=1}^{N} e^{-j\,(K-1)w} S_K(Nw)$$

where L represents the number of filter branches and w the frequency defined as follows: $2\pi f/F$, and $S_K(w)$ the frequency responses of N real digital filters 18, preferably all-pass filters that are to be specified in the design of the polyphase filters 6. The design of the prototype low-pass filters shows that the all-pass filters can always be represented as the product of first-order sections. By shifting the prototype low-pass filter by the frequency $L*F_c$ the frequency response of a complex band-pass filter $H_L(w)$ is obtained that takes over the generation of an analytical bandpass signal:

$H_L(w) = H(w-2\pi LF_c/F) = H(w-2\pi L/N)$. If the periodicity of the real all-pass functions S_k in 2π, then the following is obtained:

$$H_L(w) = 1/N \sum_{K=1}^{N} e^{-j\,(K-1)w} S_K(Nw)\, c_K$$

where the N constants (C_K) are given by $C_K = e^{j2\pi(K-1)L/N}$ for K = 1, ..., N. The complex bandpass filter can be realized with the aid of additional complex multipliers or, as shown in Figure 1 or 2, constructed with the aid of a central processor 8. The all-pass filters of the polyphase filter 6 are clocked at the second sampling rate F_c. This is possible, since the all-pass filters of the prototype low-pass filter, and therefore also those of the complex bandpass filter, operate with delays of N x T_c, where $T_c = 1/F_c$.

A digital filter structure is thus employed which carries out the arithmetical operations exclusively at the second clock frequency F_c. The time-sampled signal is converted into a series of digital numbers with the aid of the A/D converter 2. In this case the A/D converter 2 operates at the first clock frequency F that is provided by the clock generator 3. The series of digital numbers is fed to a multiplexer 5, which, as Figure 2 shows, distributes these to the all-pass filters of the polyphase filter 6. Here one digital number of the series is fed to each of the N all-pass filters of the polyphase filter 6 in each cycle of the second clock frequency F_c.

The digital numbers of the series are distributed to the all-pass filters in chronological order. After filtering, the filtered digital numbers of the all-pass filters of the polyphase filters 6 are passed to a demultiplexer 7, which arranges the filtered digital numbers according to their original chronological order and passes them to the central processor 8. The central processor 8 now multiplies the filtered digital numbers according to their chronological order, depending on which all-pass filter filtered the number, with the corresponding factor c_K which is determined as follows:

$c_K = e^{j2\pi(K-1)L/N}$, where the control variable K designates the corresponding all-pass filter and ranges from 1 to N, where N designates the number of all-pass filters and the constant L was set at 1.

The constant N which sets the ratio between the first sampling frequency F and the second sampling frequency F_c according to formula (1), and the constant *m* which according to formula (2) sets the relationship between the centre frequency F_0 of the real bandpass signal and the first sampling frequency F, and the constant L which sets the shift of the complex bandpass filter to a multiple of the second clock frequency F_c, and

thus specifies the choice of channel, is input via the input unit 10.

The use of such a polyphase filter determines the filtered spectrum shown in Figure 4d from the spectrum shown in Figure 4b. Finally, by allowing for the under-sampling with the factor N, the complex baseband signal is obtained at the second clock frequency F_c, as shown in Figure 4e.

Complex multipliers can also be provided instead of the central processor 8, that is connected to the memory 9. The complex multipliers, that have access to memories in which the factors C_K are stored, multiply the filtered digital numbers by the factors C_K. The digital numbers multiplied by the factors C_K are then added so that the digital numbers filtered by all-pass filters with odd control variable are added to a first sum and the numbers filtered by all-pass filters with even control variable are added to a second sum, the first sum representing the in-phase components and the second sum the quadrature components of the baseband signal. The in-phase components are formed by the real part and the quadrature components by the imaginary part of the sum.

A particularly important special case for implementation is illustrated in Figure 3. Here the constant N is made a multiple of four and the constant L is set to a quarter of N. In this case the coefficients c_K are given by: $C_K = e^{j\pi(K-1)/2} = j^{K-1}$, where the control variable K ranges from 1 to N, i.e. the coefficients c_K assume the values j, -j or 1, -1. Multiplication with these coefficients can therefore be carried out without multipliers. In this case the complex bandpass filter can be made a purely real one. The paths for which C_K is real form the in-phase components by addition/subtraction. Those for which C_K is imaginary, accordingly form the quadrature components. In this case the complete complex bandpass filter can therefore be made a purely real one.

In this case the formula (2) reads: $F_0 = mF + (L/N)\ F = mF + F/4$. If the constant *m* is made zero, then the known "quarter period sampling", i.e. $F_0 = F/4$. As Figure 3 shows, the digital numbers filtered by the four all-pass filters 22, 23, 24, 25 are fed to the first and second adder 11, 12 and the in-phase and quadrature components of the baseband signal are obtained by simple addition.

Allowance should be made for the fact that the digital number filtered by the first all-pass filter 22 is fed to the first adder 11 and the digital number, given a negative sign, which is filtered by the third all-pass filter 24 is also supplied to the first adder 11. The first adder 11 generates a sum from the digital numbers thus supplied, which represents the in-phase components of the baseband signal. The digital number filtered by the second all-pass filter 23 is fed to the second adder 12 and the digital number filtered by the fourth all-pass filter 25 is given a negative sign and is fed to the second adder 12. The second adder 12 generates a sum from the two digital numbers thus supplied, which represents the quadrature components of the baseband signal.

An important advantage of the proposed process is that DC voltage offsets of the A/D converter 2 which are unavoidable in practice, are completely suppressed by the digital filter since the complex bandpass filter in principle has an attenuation peak at the frequency F = 0. Of course this only applies if adjacent channel rejection is possible, i.e. when the constant N is made greater than or equal to 3.

Suppression of undesirable in-phase and quadrature components of about 57 dB is achieved by the process described in the example. Adjacent channel rejection is approximately 49 dB.

Digital frequency correction (AFC) is frequently added to the generation of in-phase and quadrature components in digital baseband systems. Here the complex baseband signal is

multiplied by a complex series: $So(n) = e^{-j2\pi n\, \Delta f/Fc}$, where the control variable n represents the clock, Δf a frequency deviation determined from the optimum frequency, and j the imaginary unit.

Since in the general case the polyphase filter 6 used to generate the in-phase and quadrature components requires complex multipliers, it is advantageous to effect the frequency correction inside the polyphase filter. Here the factors c_K are multiplied by the complex series $S_O(n)$ prior to the multiplication by the filtered digital numbers. It is advantageous to determine the complex series $c_K * S_O(n)$ recursively with a loop having a time delay of the second frequency cycle T_C, and a modulo 2 adder as illustrated in the block diagram of Figure 5.

The construction of the digital filter shown in Figure 5 makes it possible to achieve an immediate channel change with the aid of coefficients O_K employed during the determination of the coefficients C_K, by varying the whole number constants L. Since according to the equation (3) only the values between (N-1)/2) and ((-N-1)/2) are permissible for the constant L, the number of selectable channels is ((N-1)/2). If the constant N is even, ((N/2)-1) different channels can thus be selected. If the constant N is odd, there are ((N-1)/2) channels. The centre frequencies of the various channels are given by the equation (2). In this case it must therefore be assumed that the spacings of the channel centre frequencies are equal to the second clock frequency F_c. Since the proposed channel changeover does not involve transient phenomena, this arrangement is offered for use in "frequency-hopping" systems, in particular.

Claims

1. Process for the digital generation of a complex baseband signal, whereby a real baseband signal was sampled by a sample-and-hold device (1) at a first clock frequency (F) and the sampled baseband signal was transformed into a series of digital numbers with the aid of an A/D converter (2), the series of digital numbers is fed to a recursive polyphase filter (6) having a specified transfer function (H(w)), that consists of a specified number (N) of filters (18), and the specified number (N) of digital numbers is fed to the polyphase filter (6) in each cycle, and a digital number is filtered by each filter (18) of the polyphase filter (6), and the filtered numbers are then added, **characterised in that** the filtering of the digital numbers by the filters (18) of the polyphase filter (6) is carried out at a second clock frequency (F_C) that is calculated from the first clock frequency (f) by division by the number (N) of filters (18), that prior to addition, each filtered number is multiplied by a factor (c_K) that results from the frequency shift of the polyphase filter (6).

2. Process according to Claim 1, **characterised in that** the factor (c_K) is specified by the relationship: $c_K = e^{j2\pi(K-1)L/N}$, where the control variable K designates the Kth filter (18) of the polyphase filter (6), the constant N designates the number of filters (18), the whole-number constant L designates the frequency shift of the polyphase filter (6) by L units of the second clock

frequency F_C and the value of the constant L lies between 1 and [N-1]/2 and *j* represents the imaginary unit.

3. Process according to one of the Claims 1 or 2, **characterised in that** the number (N) of filters (22, 23, 24, 25) is set to a multiple of 4 and the constant (L) to a quarter of the number (N) of filters (22, 23, 24, 25), and that the numbers filtered by the filters (22, 24) with even control variable K are added to a first sum and the numbers filtered by the filters (23, 25) with odd control variable K are added to a second sum in the second frequency cycle (T_C), whereby the first sum represents the in-phase components and the second sum the quadrature components of the real baseband signal.

4. Process according to one of the Claims 1 to 3, **characterised in that** the sampling frequency F_0 of the baseband signal, the sampling frequency F and the sampling frequency of the complex baseband signal F_C are specified so as to fulfil the following relationships: $F = N * F_C$ and $F_0 = m * F + L * F_C$, where *m* and L are specified whole-number constants.

5. Process according to one of the Claims 1 to 4, **characterised in that** the filters (18, 22, 23, 24, 25) of the polyphase filter (6) are constructed as all-pass filters.

6. Process according to one of the Claims 1 to 5, **characterised in that** prior to multiplication with the filtered numbers corresponding to the second frequency cycle ($T_C = 1/F_C$), the factors (c_K) are multiplied by a complex series $S_0(n) = e^{-j2\pi m\Delta f/F_c}$, where Δf represents a determined frequency deviation, the control variable (n) the clock and the constant (j) the imaginary unit.

7. A process for the digital generation of a complex baseband signal substantially as herein described with reference to the accompanying drawings.

Patents Act 1977 Examiner's report to the Comptroller under Section 17 -17- (T Search report)	Application number GB 9418023.9
Relevant Technical Fields (i) UK Cl (Ed.M) H4P (PAD, PAFC, PAFX, PAL, PAQ, PAX, PRE) (ii) Int Cl (Ed.5) H03H 17/04, 21/00; H03K 4/02; H04B 14/00; H04L 25/03, 25/06, 25/08, 27/12. 27/20, 27/36	Search Examiner MR K WILLIAMS Date of completion of Search 9 NOVEMBER 1994
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE DATABASE: WPI	Documents considered relevant following a search in respect of Claims :- 1-7

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